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ROC920030248US1

R E M A R K S

- Claims 1 to 20 are pending
- Claims 1 and 10 are the only pending independent claims

The Examiner objected to the specification based upon the assertion that the title is not descriptive. Applicants have herein amended the title to be more descriptive and respectfully request withdrawal of the specification objection based upon the new title.

The Examiner rejected Claims 1 to 20 under 35 U.S.C. 102(b) as being anticipated by Garreau (U.S. Patent No. 6,425,101). Applicants respectfully traverse the rejection.

Applicants' claims are directed to methods and apparatus for testing an integrated circuit (IC) that includes using multiple input and output (I/O) lines so that if a test of an IC is unsuccessful, alternative I/O lines may be used to retry the test. By retesting using different I/O lines, the present invention provides an indication whether the test was unsuccessful due to the I/O lines or due to the IC.

In contrast, the Garreau reference describes a network architecture (referred to as a "crossbar" switch) that appears to allow selective testing of ICs connected to the network. There is no disclosure (or even suggestion) identified by the Examiner or that Applicants can find within Garreau wherein the network includes multiple alternative I/O lines to and from a single IC, much less a teaching to try different combinations of the alternative I/O lines if a test of the IC is unsuccessful.

More specifically, Applicants' independent Claim 1 recites:

> if the test result is unsuccessful, performing at least one of:
>
> employing a remaining one of the plurality of input lines to receive the test signal for the processor; and
>
> employing a remaining one of the plurality of output lines to send the test result from the processor.

Independent Claim 10 recites a similar feature. Despite the Examiner's assertion to the contrary, no where in Garreau is such retesting described. The Examiner attempts to support his rejection based on FIG. 4 and the associated text of Garreau. However, Garreau's FIG. 4 merely depicts "a programmable switch" and the associated text only states:

> Referring now to FIG. 4, an illustration of a programmable switch 400 in accordance with an embodiment of the invention is shown. It should be noted that the programmable switch 400 is but one possible embodiment of the programmable switch 204 shown in FIG. 2. The programmable switch 400 includes vertical data lines 402 programmably connected to horizontal data lines 404 forming what is referred to as a "crossbar" switch. The vertical data lines 402 and horizontal data lines 404 can be selectively electrically connected to each other using programmable connectors to provide a signal path suitable for passing control signals and data signals. It should be noted that for sake of clarity, only a few of the available programmable connectors are shown and that in practice a programmable connector is located at every horizontal and vertical data line intersect. The vertical data lines 402 are connected to a vertical data line controller 406 which is connected to the switch controller 218 while the horizontal data lines 404 are connected to a horizontal data line controller 408 also connected to the switch controller 218. Each of the horizontal data lines 404 is connected to one of the programmable switch I/O lines 410. Each of the programmable switch I/O lines 410 are in turn connected in a pair-wise manner to the integrated circuits IC1 through IC4 located on the target hardware device 206. By way of example, a horizontal data line 404-1 is connected to a programmable

> switch I/O line 410-1 while a horizontal data line 404-2 is connected to a programmable switch I/O line 410-2. Continuing the example above, the I/O lines 410-1 and 410-2 are, in turn, connected to the feed forward line 220 and the feed backward line 222.
>
> In order to selectively connect the IC1 to the JTAG controller 210, the horizontal data line controller 408 uses programmable connectors 412-1 and 412-2 to connect the horizontal data line 404-1 to the vertical data line 402-1 and the horizontal data line 404-2 to the vertical data line 402-2. The vertical data line controller 406 uses the programmable connector 412-3 to connect the vertical data line 402-1 to the JTAG controller 210 by way of the I/O line 211-1. The vertical data line controller 406 then uses the programmable connector 412-4 to connect the vertical data line 402-2 to the JTAG controller 210 by way of the I/O line 211-2. In this way, a test feedback loop is formed between the JTAG controller 210 and the integrated circuit IC1. At this point, the master controller 202 can direct the JTAG controller 210 to execute the appropriate JTAG test protocols associated with the integrated circuit IC1 (or proprietary OCDS transactions).

Thus, it is clear that Garreau does not teach or even suggest Applicants' above-quoted feature of independent Claims 1 and 10. At most, FIG. 4 and the associated text appears to simply show a method for testing an integrated circuit using the crossbar switch to selectively connect to the IC. There is absolutely no mention of retesting if a test is unsuccessful, much retesting using alternative I/O lines. Thus, Applicants' claimed invention is not anticipated by the reference since Garreau fails to teach or suggest every element of the claimed invention. Claims 2 to 9 and 11 to 20 directly or indirectly depend on Claims 1 or 10, respectively. Thus, Applicants respectfully request that the Examiner reconsider and withdraw the section 102 rejection.

Please charge Deposit Account No. 04-1696 for any fees required by this Amendment. The Applicants

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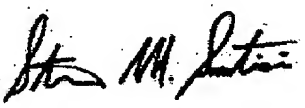
encourage the Examiner to telephone Applicants' attorney should any questions remain.

Respectfully Submitted,



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